

Date of publication xxxx 00, 0000, date of current version xxxx 00, 0000.

Digital Object Identifier 10.1109/ACCESS.2017.Doi Number

An improved LCL-L Compensation Topology for Capacitive Power Transfer in Electric Vehicle Charging

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This work was supported in part by the Newcastle-Singapore research scholarship.

ABSTRACT This paper proposes an LCL-L compensation circuit for high power capacitive power transfer (CPT) aiming at minimizing number of resonant components and improving system performance. The proposed topology adopts only four external resonant components at both sides of the capacitive coupler. The output power is proportional to the capacitive coupling coefficient, therefore, it simplifies the design procedure and abolishes protection circuit requirements under coupler's misalignment. Moreover, optimizing efficiency at full-load conditions of compensation network can be easily achieved in this system by designing resonant components at the highest value of the mutual capacitance. Theoretical analysis of the proposed system is conducted alongside comparison to lasted CPT compensation circuits. Simulation and experimental results of a 1.5-kW CPT prototype with an air gap distance of 150 mm are provided to verify the feasibility and the effectiveness of the proposed system. System performances under different coupler's misalignment conditions and output power levels are also examined and discussed as well.

INDEX TERMS Capacitive power transfer, Compensation circuits, LCL-L topology, Electric Vehicles, Battery Charger.

I. INTRODUCTION

As compared with an Inductive Power Transfer (IPT) system, a capacitive power transfer (CPT) system has several benefits such as implementing low-cost and insensitive to nearby metal objects [1]. The developments of contactless CPT systems for low power and low air-gap applications such as consumer electronics, LED lighting, battery charging have been received the most attention [2-13]. The single series inductor is normally added into either one side or both sides of capacitor plates to compensate for the high leakage capacitances [2-4]. The CPT system and the associated compensation circuits for multiple pickups constant current output applications are presented in [5]. To prevent the electrical and health hazards when the secondary side load is removed suddenly, the different design approaches of the compensation networks are discussed in [6-8]. In addition, different methods are introduced in [9, 10] to reduce the high voltage stresses among the capacitor coupler plates and compensation components. To simplify the capacitive coupler structure, the CPT systems with only two coupling

plates are proposed in [12,13]. The output power in several CPT systems can be increased to kilowatt scales for applications such as contactless stationary EVs charging [14, 15] or dynamic EVs charging [16].

However, the CPT technology has still not been widely used in high power and large air-gap applications due to its limitation of low mutual capacitance. When the air-gap reaches to around 15-20 cm for applications such as Electric Vehicle battery charging (i.e. illustrated in Fig. 1), then mutual capacitance values between two coupling plates reduces to picofarad range [21]. Consequently, it requires very large inductors in the compensation circuit if simple series compensation topologies are used [2-3]. Low mutual capacitance also results in very large voltage stresses on resonant inductors. In terms of energy conversion, high efficiency is very difficult to achieve at low coupling capacitance condition.

In order to address the above issues, several solutions have been proposed recently. The first solution utilizes wide-bandgap semiconductors (SiC/GaN) to operate the CPT

charger at high frequency for compensating the low mutual capacitance and achieving high power density [17,18]. Most of the recent CPT systems operate at a frequency of greater than 1 MHz. In [18], the new design method of the 6.78-MHz CPT system is proposed to mitigate the negative effect of parasitic elements. The second approach uses the multi-modular architecture to achieve high power transfer while maintaining the safety limits [19, 20]. Therefore, the total output power is summed up from each module's power. However, this approach increases the component counts consisting of power electronics converters as well as coupling capacitor plates and resonant networks.

The third method focuses on the resonant network by utilizing new compensation topology to upgrade the output power under low mutual capacitance conditions [21-25]. These papers proposed adding extra capacitors connected in parallel with the capacitive coupler at both sides to solve the low coupling capacitance problem. Combining with recent advancement in power semiconductor devices, in which high frequency and high-power switches are available, the CPT compensation circuit can be realized at higher than 1 MHz switching frequency. In [21], a double-sided LCLC topology is proposed to transfer 3 kW power with 15 cm air-gap and achieving 90.8% efficiency. As mentioned in [21], an additional 100-pF capacitor was connected in parallel with 231- μ H series inductor at both sides to operate at 1 MHz of switching frequency. However, there are eight external components in the compensation circuit, reducing the system's compactness and increasing the implementation cost. In order to reduce the number of components and coupler's installation space, a four-plate structure for the capacitive coupler is proposed in [22]. The system in [22] used two separated pairs of metal, which are vertically integrated to reduce the space. Moreover, two extra parallel capacitors in [21] can be replaced by adopting two large coupling capacitors of two plates that are on the same side in [22]. Double-sided LCLC topology in [21] can be simplified as double-sided LCL in [22] with only six external components. To further reduce the number of components, double-sided LC topology [23, 24] is proposed by developing from a series compensation circuit where only an external inductor and capacitor are connected in series and parallel with the capacitive coupler in each side respectively.

In both [21] and [22], the output power is proportional to the capacitive coupling coefficient k , which brings several advantages. Firstly, the highest efficiency point is normally preferred at the full load condition in power converter system to reduce total losses [26]. Hence, the CPT system can attain the highest efficiency by designing compensation circuit of CPT system at full load and highest value of k , meaning at perfectly alignment case. Secondly, overpower protection circuit is not required in any misalignment case, as output power is also degraded when k decreases. However, the output power in the case of double-sided LC topology [23-24] is reversely proportional with k and it is only a function

of the switching frequency and the capacitive coupler value. Consequently, it is very difficult to a design compensation network for achieving high efficiency at the full load condition and furthermore, the protection requirement is a must if misalignment occurs. This also reduces flexibility to design the capacitive coupler for attaining a relatively large coupling coefficient resulting in better system efficiency.

This paper introduces the LCL-L compensation circuit topology (i.e. illustrated in Fig. 2) for high power and large air-gap CPT systems such as Electric Vehicle battery charging to eliminate the abovementioned drawbacks associated with double-sided LC topology. The first feature of the proposed topology is that only four external components are required, which is similar to the topology presented in [23-24]. An LCL compensation network is connected at the primary side and an inductor is connected in series with capacitive coupler at the secondary side. Secondly, the output power is proportional to capacitive coupling coefficient, which brings several benefits in terms of design and protection aspects. Differentiating from the existing work [7], in which the authors have only focused on design of the compensation network for the movable devices with low output power and small air-gap, a design guideline of a LCL-L compensation network is given in this paper for the stationary electric vehicle battery applications with high output power (i.e. 1.5 kW) and large air-gap (i.e. 15 cm).

The theoretical analysis is provided, and relevant equations are derived to achieve the above features. The relationship between the output voltage, power and coupling coefficient is presented, where conditions to attain near Zero-Phase-Angle (ZPA) and Zero Voltage Switching (ZVS) conditions of primary inverter are investigated. A flowchart of the detailed design procedure is illustrated alongside with simulation results. Comparison is presented between doubled-side LCLC presented in [21, 22], doubled-side LC reported in [23, 24] and the proposed LCL-L topologies, considering the number of external components and output power characteristics. A laboratory prototype of 1.5-kW CPT is developed to experimentally validate the proposed topology. The performance of the proposed circuit topology is further examined under misalignment and different load conditions.

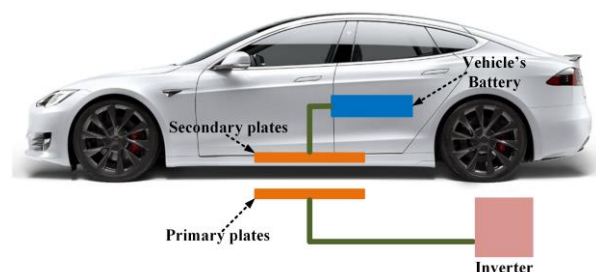


FIGURE 1. A Capacitive charger system for Electric Vehicles.

II. PROPOSED LCL-L COMPENSATION TOPOLOGY CPT SYSTEM

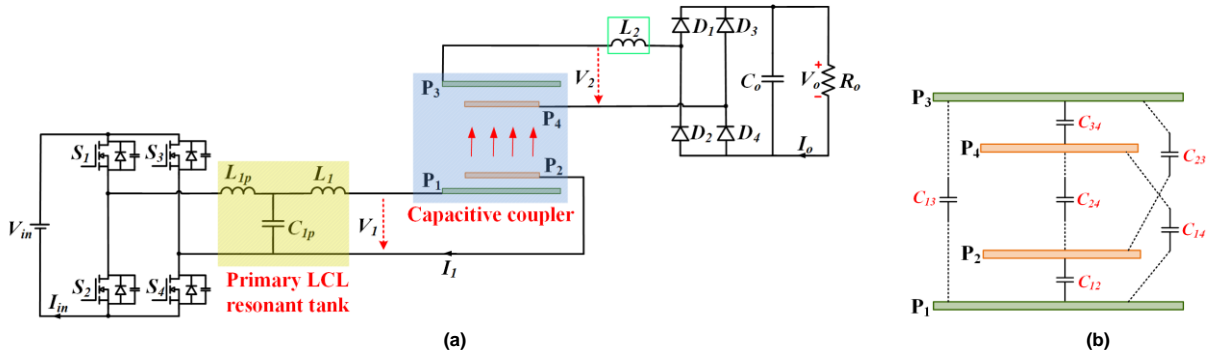


FIGURE 2. (a) The proposed LCL-L topology for capacitive power transfer, (b) Structure of the capacitive coupler

A. OPERATING PRINCIPLE

Figure 2a illustrates the proposed LCL-L compensation topology for CPT, which comprises a full-bridge inverter at the primary side, compensation networks in both sides, capacitive coupler with integrated structure [22] and a bridge rectifier at the secondary side. CPT system is energized by a DC Voltage source V_{in} to provide a DC power for an output battery load, which in this case is simply represented by resistive load, R_o , for simplicity. V_o and I_o are the required output voltage and output current, respectively. In this paper, the First Harmonic Approximation (FHA) is used to analyze the proposed system in the frequency-domain for simplicity. Therefore, first harmonic components can be derived from the equivalent circuit of Fig. 3 as given by (1). Therefore, v_{in_AC} , v_{o_AC} and i_{o_AC} in (1) are the first harmonic components of the input voltage, output voltage and current of the compensation circuit, respectively. In the following analysis V_{in} , V_1 , V_2 , V_o , I_{in} , I_1 , and I_o are used to express the complex form of the corresponding variables.

$$\begin{cases} v_{in_AC}(t) = \frac{4}{\pi} V_{in} \sin(2\pi ft) \\ v_{o_AC}(t) = \frac{4}{\pi} V_o \sin(2\pi ft + \theta) \\ i_{o_AC}(t) = \frac{\pi}{2} I_o \sin(2\pi ft + \theta) \\ R_{AC} = \frac{8}{\pi^2} \frac{V_o}{I_o} = \frac{8}{\pi^2} R_o \end{cases} \quad (1)$$

As it can be noticed from Fig. 2 (a) and (b), the capacitor between plates P_i and P_j is given by C_{ij} ($i, j = 1, 4$). The coupling capacitors C_{12} and C_{34} are adopted to form two extra parallel capacitors, which use to boost the voltage supplied for capacitive coupler. The value of C_1 , C_2 and C_M are depicted in (2) according to [22].

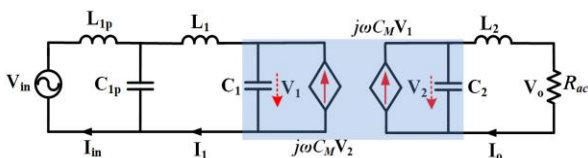


FIGURE 3. Equivalent circuit model of LCL-L compensation topology

$$\begin{aligned} C_1 &= C_{12} + \frac{(C_{13} + C_{14})(C_{23} + C_{24})}{C_{13} + C_{14} + C_{23} + C_{24}} \\ C_2 &= C_{34} + \frac{(C_{13} + C_{23})(C_{14} + C_{24})}{C_{13} + C_{14} + C_{23} + C_{24}} \\ C_M &= \frac{C_{24}C_{13} - C_{14}C_{23}}{C_{13} + C_{14} + C_{23} + C_{24}} \end{aligned} \quad (2)$$

At the secondary side, the voltage loop can be expressed by Eqs (3-4).

$$I_o = j\omega C_M V_1 - j\omega C_2 V_2 \quad (3)$$

$$V_o = V_2 - j\omega L_2 I_o = (1 - \omega^2 L_2 C_2) V_2 + \omega^2 L_2 C_M V_1 \quad (4)$$

$$1 - \omega^2 L_2 C_2 = 0 \quad (5)$$

In order to simplify the control of V_o , L_2 and C_2 should form a series resonance as shown in (5). Therefore, the output voltage directly depends on the mutual capacitance between the two sides, C_M and the voltage value on equivalent primary capacitor V_1 . Moreover, V_1 in the CPT system plays a similar role as the transmitter coil current in the IPT system [27]. Similarly, to simplify the control of output voltage, the value of V_1 should be maintained constant regardless of load condition at the secondary side. At the primary side, the relationship between V_{in} and V_1 can be expressed as follows:

$$\begin{aligned} V_1 &= V_{C1p} + V_{L1} = (I_1 - I_{in}) \frac{1}{j\omega C_{1p}} - j\omega L_1 I_1 \\ &= \left(\frac{1}{j\omega C_{1p}} - j\omega L_1 \right) I_1 - \frac{1}{j\omega C_{1p}} I_{in} \end{aligned} \quad (6)$$

$$\begin{aligned} V_{in} &= j\omega L_{1p} I_{in} + (I_{in} - I_1) \frac{1}{j\omega C_{1p}} \\ &= \left(j\omega L_{1p} + \frac{1}{j\omega C_{1p}} \right) I_{in} - \frac{1}{j\omega C_{1p}} I_1 \end{aligned} \quad (7)$$

where V_{C1p} and V_{L1} are voltage on C_{1p} and L_1 respectively.

Similar to the primary LCC topology in IPT systems [28], the L_{1p} and C_{1p} form a resonant circuit and function as an input filter, which removes high-order harmonics from the current injected to primary plates. Furthermore, their resonance makes

I_1 constant regardless of the load condition. As a result, I_1 can then be derived as (8) with the condition presented in (9).

$$I_1 = -j\omega C_{1p} V_{in} = \frac{1}{j\omega L_{1p}} V_{in} \quad (8)$$

$$j\omega L_{1p} + \frac{1}{j\omega C_{1p}} = 0 \quad (9)$$

From (6), to keep V_1 independent of load condition, then $1/(\omega C_{1p})$ should be very small as compared to ωL_1 . Eq. (10) expresses V_1 under this constraint combining with (8).

$$V_1 \approx -j\omega L_1 I_1 = -\frac{L_1}{L_{1p}} V_{in} \quad (10)$$

Therefore, the output voltage of the proposed topology is independent of the load condition and is proportional with a coupling capacitor between the two sides. Eqs. (11) and (12) depict V_o and output power P_o while I_o is the output battery current, which is a function of the load condition. Consequently, P_o is also proportional to the coupling capacitor C_M . It is noted that the phase of output voltage V_o and input voltage V_{in} are reversed. In other words, the phase-shift θ in (1) between V_o and V_{in} is 180° .

$$V_o \approx -\omega^2 L_2 C_M \frac{L_1}{L_{1p}} V_{in} \quad (11)$$

$$P_o = V_o I_o \approx \omega^2 L_2 C_M \frac{L_1}{L_{1p}} V_{in} I_o \quad (12)$$

The input impedance for CPT system Z_{in} can be derived from the equivalent circuit depicted in Fig. 2 in the same way as the IPT system, where the phase angle of Z_{in} indicates the phase difference between V_{in} and I_{in} . To minimize the losses and stresses on the primary inverter, the phase angle of Z_{in} should be positive and close to zero to achieve soft-switching turn-on for MOSFETs of the primary inverter [22]. This section explores the conditions to attain Zero-Phase-Angle (ZPA) of Z_{in} . Fig. 3 shows the simplified model of Fig 2 where Z_S represents the secondary circuit's impedance and Z_R is the reflection of Z_S to the primary side as expressed in (13).

$$Z_S = \frac{V_2}{j\omega C_M V_1} = \frac{\frac{1}{j\omega C_2} (j\omega L_2 + R_{ac})}{\frac{1}{j\omega C_2} + j\omega L_2 + R_{ac}} \quad (13)$$

$$Z_R = \frac{V_1}{-j\omega C_M V_2} = \frac{1}{\omega^2 C_M^2 Z_S} \quad (14)$$

Therefore, the input impedance of the proposed system, Z_{in} can then be written as (15), considering the resonant operation condition described by (5) and (9).

$$\begin{aligned} Z_{in} &= \frac{j\omega L_{1p}}{1 + j\omega C_{1p} \left(j\omega L_1 + \frac{Z_R}{1 + j\omega C_1 Z_R} \right)} \\ &= \frac{j\omega L_{1p} (1 + j\omega C_1 Z_R)}{1 - \omega^2 C_{1p}^2 + j\omega Z_R (C_1 + C_{1p} - \omega^2 C_1 C_{1p} L_1)} \end{aligned} \quad (15)$$

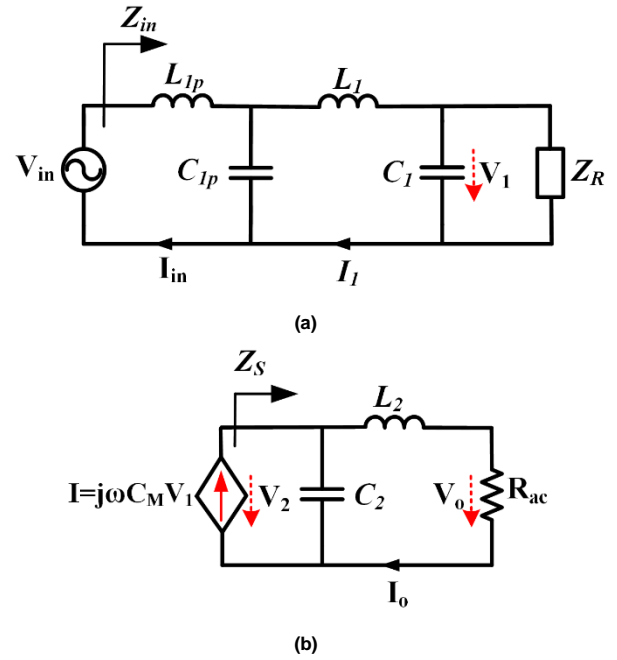


FIGURE 4. Simplified equivalent circuit of Fig. 3 (a) Primary side, (b) Secondary side

To further simplify Z_{in} , another resonant loop at the primary side, between C_1 , C_{1p} , and L_1 should be formed, which is described by (16). Therefore, the simplified version of Z_{in} is given by (17).

$$j\omega L_1 + \frac{1}{j\omega C_1} + \frac{1}{j\omega C_{1p}} = 0 \quad (16)$$

$$\begin{aligned} Z_{in} &= \frac{1}{(1 - \omega^2 L_1 C_{1p}) C_M^2 (\omega^2 L_2^2 + R_{ac}^2)} [\omega^2 C_1 C_2 L_{1p} L_2 R_{ac} \\ &\quad + j\omega L_{1p} (\omega^2 L_2^2 C_M^2 + C_1 C_2 R_{ac}^2)] \end{aligned} \quad (17)$$

Hence, the phase angle of Z_{in} can be calculated as follows:

$$\begin{aligned} \varphi(Z_{in}) &= \tan^{-1} \left[\frac{\text{Im}(Z_{in})}{\text{Re}(Z_{in})} \right] \\ &= \tan^{-1} \left[\frac{\omega^2 L_2^2 C_M^2 + C_1 C_2 R_{ac}^2}{\omega C_1 C_2 L_2 R_{ac}} \right] \end{aligned} \quad (18)$$

The design procedure in this paper neglects the term $\omega^2 L_2^2 C_M^2$ as compared to $C_1 C_2 R_{ac}^2$. Therefore, $\varphi(Z_{in}) \approx \tan^{-1} \left(\frac{R_{ac}}{\omega L_2} \right)$, this can be noticeable that $\varphi(Z_{in})$ is always positive. MOSFETs of the primary inverter are turned on at a zero-voltage switching (ZVS) condition. Furthermore, R_{ac} can be calculated according to load requirement while the switching frequency can be maintained at around 1-MHz. Therefore, L_2 should be selected for ωL_2 to be large enough as compared to R_{ac} . This constraint guarantees the near ZPA operation for the primary inverter.

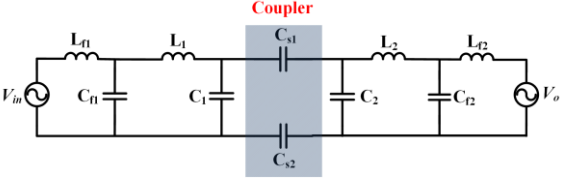
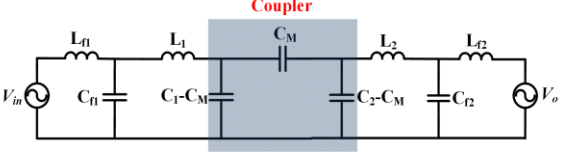
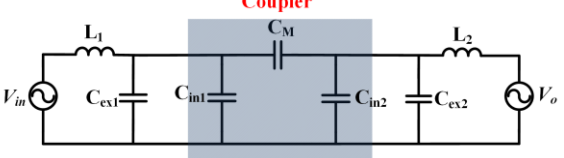
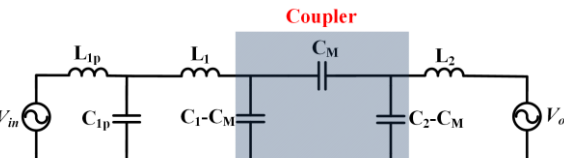
B. COMPARISON BETWEEN CPT COMPENSATION TOPOLOGIES

In this section, doubled-side LCLC, doubled-side LC, and the proposed LCL-L topologies are compared to each other, considering the following aspects: (a) the number of external components (b) output power characteristic (c) efficiency at rated power and (d) design flexibility. This is summarized in Table I below. As demonstrated by Table I, minimizing the number of components is an important feature of double-sided LC and the proposed LCL-L topology in which each topology only requires four external components, in addition, the coupling capacitors. Smaller number of components, lower implementation cost, and higher power density. The second factor is the output power, which is inversely proportional to the mutual capacitance C_m in the case of double-sided LC topology while it is proportional to C_m for both, the double-sided LCLC and the proposed LCL-L. Design compensation circuits necessitate that the highest value of P_o must correspond to the highest value of C_m . This is to guarantee that maximum efficiency can be attained at the highest output power point. On the other hand, when misalignment occurs, C_m drops below certain range and the input power exceeds the limited value, therefore overpower protection is essential for double-sided LC to stop charger while double-sided LCLC and the proposed topology do not require one as output power is proportional with C_m .

Moreover, if the protection circuit is not required, then C_m must be reduced in order to increase the power level of the system, resulting in lower efficiencies at heavy loads. In double-sided LCLC and the proposed topology, efficiency optimization is easier as it only needs to design the highest P_o value when C_m reaches maximum value (no misalignment). However, if misalignment occurs, C_m is reduced with reduction of P_o . Efficiency will be also dropped, however, at a lower level of output power.

Another factor is the system flexibility in designing the capacitive coupler. As shown in Table I, the output power can be regulated by adjusting the ratio between $C_{f1}C_{f2}$ and C_1C_2 in an LCLC-compensated CPT system. Similarly, in the proposed topology, the output power can also be adjusted by varying the values of L_1 , L_2 and L_{1p} when coupling capacitors are fixed. This feature provides the flexibility to design the capacitive coupler to achieve a relatively large mutual capacitance C_m , hence a better system efficiency. This advantage, however, is incapable to achieve in double-sided LC topology.

TABLE I
COMPARISON BETWEEN DIFFERENT CPT COMPENSATION TOPOLOGIES

Topologies	Configuration	No. of external components	Output power
Double-sided LCLC [21] (with horizontal plates structure)		8	$P_o = \omega_o C_s \frac{C_{f1} C_{f2}}{C_1 C_2} V_{in} V_o$ where: $C_s = \frac{C_{s1} C_{s2}}{C_{s1} + C_{s2}}$
Double-sided LCL [22] (with vertical plates structure)		6	$P_o = \omega_o C_m \frac{C_{f1} C_{f2}}{(1 - k_c^2) C_1 C_2} V_{in} V_o$ where: $k_c = \frac{C_m}{\sqrt{C_1 C_2}}$
Double-sided LC [23-24] (with horizontal plates structure)		4	$P_o = \omega_o \frac{C_1 C_2}{C_m} V_{in} V_o$ where: $\begin{cases} C_1 = C_{ex1} + C_{in1} \\ C_2 = C_{ex2} + C_{in2} \end{cases}$
The proposed LCL-L (with vertical plates structure)		4	$P_o = \omega_o^2 L_2 C_m \frac{L_1}{L_{1p}} \frac{V_{in} V_o}{R_o}$ where R_o is load resistance and $R_o = \frac{V_o}{I_o}$

III. DESIGN PROCEDURE AND SIMULATION VERIFICATION

The flowchart in Fig. 5 illustrates the practical procedure for a designing compensation circuit for the proposed CPT system. First, the operating frequency needs to be designed by considering the volume and losses of resonant components as well as power switches, therefore, the frequency of 1 MHz is selected in this work. In the next step, specifications of the CPT system are determined, and equivalent load resistance is calculated based on the charging current and voltage. In the meantime, the size and geometry of the CPT coupler are determined based on the air-gap of the coupler and the limitations of the installation area. Once the coupler's dimensions are defined, then C_1 , C_2 and C_M can be estimated by using electromagnetic field simulation software such as MAXWELL 3D, while L_2 can be calculated by (5). At this point, it is also necessary to see if the set of parameters can also satisfy the conditions of $R_{ac} \ll \omega_o L_2$. If results are not satisfactory, then C_1 , C_2 and C_M need to be adjusted by varying the coupler's dimension. Value of C_M is the simulated value with 15-cm air-gap and no misalignment. The FEA simulation model and final dimensions of the capacitive coupler can be found in Fig. 6 in which the dimensions of plates P1 and P2 are identical with P3 and P4, respectively. The thickness of all four plates are the same as 2 mm. Once all the above conditions are matched, then values of L_1 , L_{1p} and C_{1p} are calculated using (9), (11) and (16). Furthermore, the specifications of the CPT charger and all other parameters are summarized in Table II. In order to verify the above analysis and design procedure, the voltage gain G_V and the phase of the input impedance Z_{in} are drawn as shown in Fig. 7.

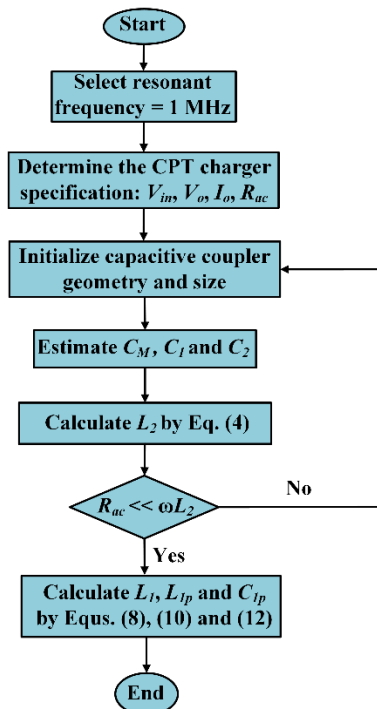


FIGURE 5. Flowchart of the proposed CPT design procedure

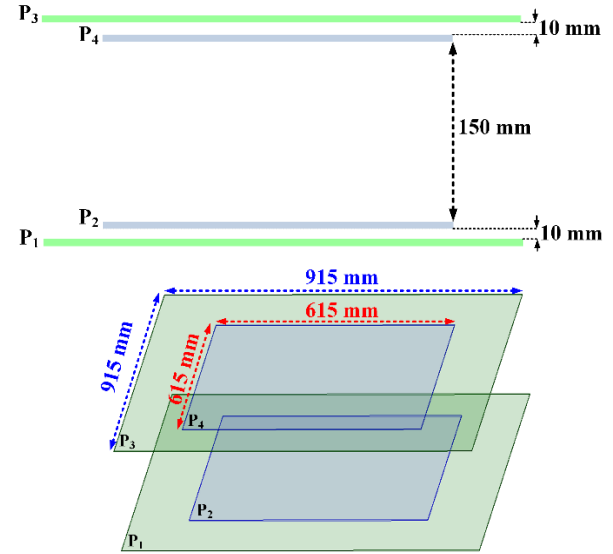


FIGURE 6. FEA model and dimensions of the capacitive coupler

TABLE II
CPT SYSTEM PARAMETERS

V_{in}	Input DC voltage	200-300 V
V_o	Output DC voltage	125 V
P_o	Rated Output Power	1.5 kW
C_1	Primary self-capacitance	380 pF
C_2	Secondary self-capacitance	380 pF
C_M	Mutual capacitance	11.5 pF
L_{1p}	Primary Additional Inductor	2.9 μ H
C_{1p}	Primary Additional Capacitor	8.73 nF
L_1	Primary Series Inductor	69.4 μ H
L_2	Secondary Series Inductor	66.5 μ H

Figure 7 shows that the voltage gain is constant regardless of the load conditions at the resonant frequency of around 1 MHz. Meanwhile, the phase angle of Z_{in} at 1 MHz is always positive and very close to zero. This confirms that the proposed topology enables the CPT system to operate in the Constant Voltage (CV) mode with near ZPA achievement. This is further confirmed by the simulation results of different load conditions as illustrated in Fig. 8. Input voltage V_{in} slightly delays with input current I_{in} and the phase-shift between them is very small, confirming that the resonant network achieves near ZPA operation. Soft-switching operation for the inverter (i.e. ZVS) is also achieved as the cut-off current at the switching transient is about 5 A. In addition, the input and output voltage are out of phase as predicted by (11). Moreover, when output power varies, the

shape of I_{in} waveform changes accordingly. As the proposal LCL-L is the voltage source, then resistive load value R_o decreases when output power increases (i.e. reduce from 40 Ω to 10 Ω in simulation). At the smallest value of R_o of 10 Ω (also the heaviest load), phase-shift between voltage and current is smallest and ZPA condition is very close. It also confirms the above condition of $R_{ac} \ll \omega_o L_2$. Phase-shift between V_{in} and I_{in} slightly increases when R_o increases as the CPT circuit goes towards to light load condition. Nevertheless, it is worth noting from Fig. 8a that the input current waveform, I_{in} is not a sinusoidal due to high harmonics. However, when the load increases then the input current becomes nearly sinusoidal at the full load (Fig. 8c). The resonance between L_{1p} and C_{1p} acts as a high-pass filter, which removes higher harmonics components at light load and provides a sinusoidal voltage and current for the primary capacitor plates.

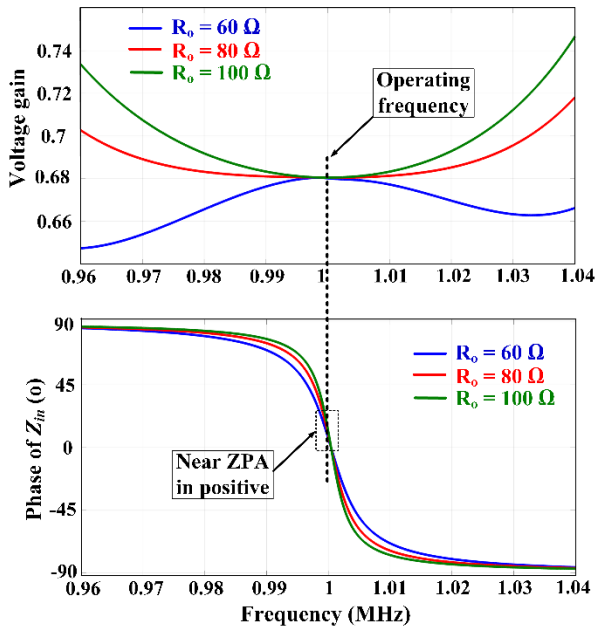


FIGURE 7. Voltage gain and phase of input impedance of the LCL-L circuit with parameters in Table II

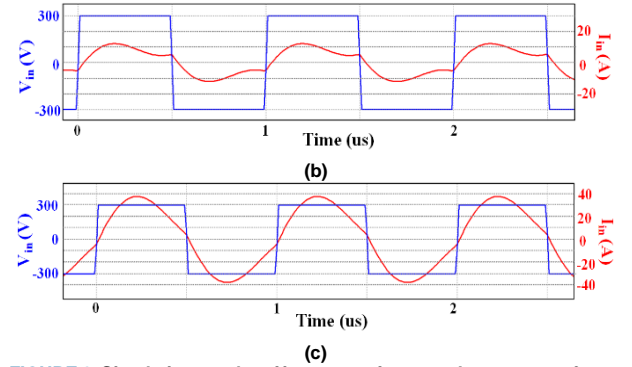
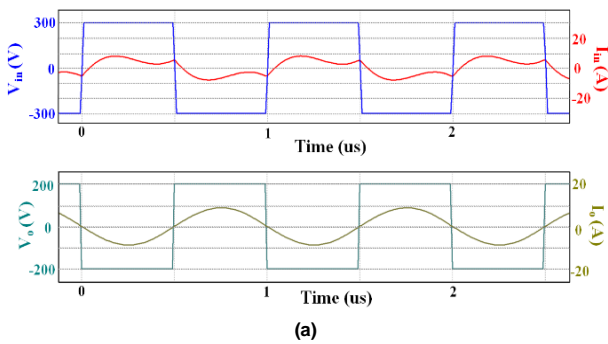


FIGURE 8. Simulation results of input waveforms and output waveforms with $V_{in}=300$ V and when the load at (a) 40 Ω and input waveforms when the load at (b) 20 Ω and (c) 10 Ω .

IV. EXPERIMENTAL VERIFICATION

Fig. 9 portrays a laboratory prototype, which was developed based on the system parameters tabulated in Table II to validate the simulation and the theoretical findings. As mentioned earlier, capacitive coupler (i.e. Fig. 9a) consists of four aluminum plates with vertical structure. All these four plates are of square shape with the dimensions of 915 mm x 915 mm and 615 mm x 615 mm for large and small plates, respectively. Fig. 9b depicts the resonant network part. High-power and high-frequency polypropylene film capacitors from TDK are used to construct the resonant capacitor C_{1p} due to their low equivalent series resistance (ESR) and high current carrying capability. All resonant inductors are constructed using Litz wire of 38 AWG to reduce the conduction losses at high frequency. To prevent potential arcing between different inductor's turns, the PVC isolation tape is wound around the copper Litz wire. The full-bridge inverter is built using low- R_{dsON} Silicon Carbide (SiC) MOSFETs (C2M0025120D from Cree) while four SiC diodes (IDW30G65C5 from Infineon) are used for the secondary full-bridge rectifier.

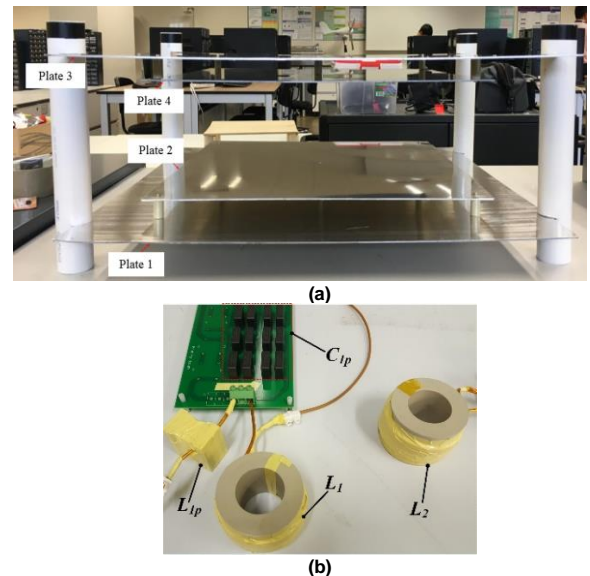


FIGURE 9. Experimental setup for the proposed LCL-L CPT charger (a) capacitive coupler (b) The resonant networks in both sides

As discussed in Section III, the rated output power is attained at the highest value of C_M when all plates perfectly aligned with 15-cm airgap. Experimental waveforms of input resonant network's voltage and current at the above condition are depicted in Fig. 10a at $R_o = 10 \Omega$ and input DC voltage of 200 V. It can be noticed that ZPA between V_{in} and I_{in} and the shape of I_{in} are in a very good agreement with the simulation results shown in Fig. 8c. At full-load condition, the output power of 1.5 kW is obtained at the secondary side for which the waveforms of output resonant network's current I_o and voltage V_o are illustrated in Fig. 10b. It should be noted that as the circuit operates at a very high frequency, then some small ringing and spikes occurred in the waveforms. However, this can be suppressed or minimized with a better design of power PCB.

Fig. 10c presents the voltage stresses on the capacitor coupler at the primary side between P1 and P2 and at the secondary side between P3 and P4. They are also equivalent to voltages V_1 and V_2 in Fig. 3, respectively, where their phase-shift is of 90 degrees. As the voltage range of probe is limit, then the waveforms are captured with an input voltage of only 100V. At full load conditions, these voltage stresses have RMS values up to 4 and 5.5 kV for primary and secondary couplers respectively. Therefore, the distance between plate P1 and P2 and between plates P3 and P4 should be large enough to avoid arcing between two plates. According to the breakdown voltage of air value, then the distance between plates is set at 1 cm for both sides in this work.

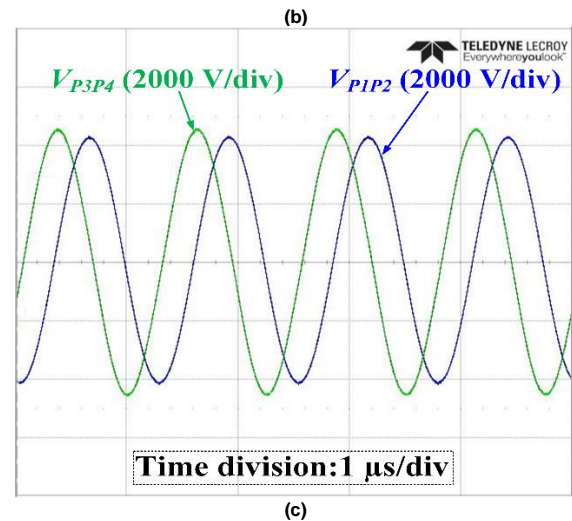
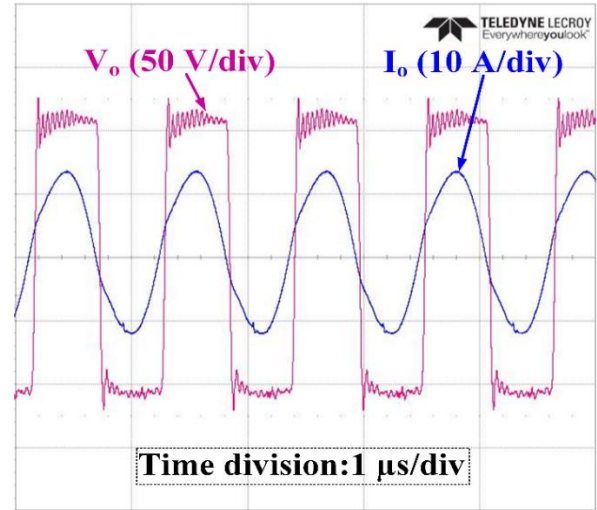
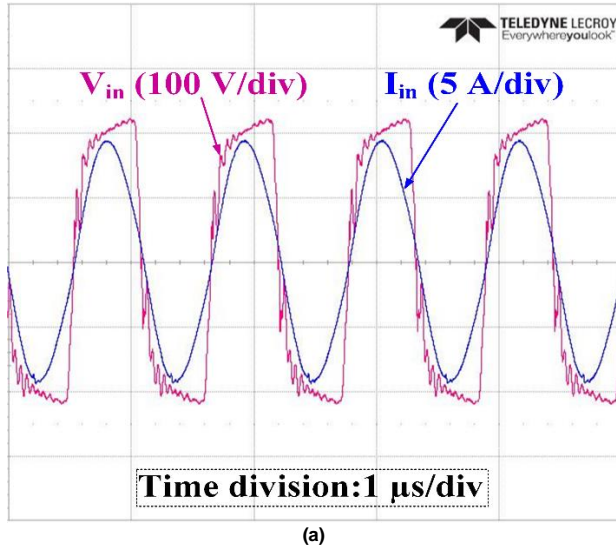


FIGURE 10. Experimental waveforms of (a) input voltage and current, (b) output voltage and current at rated load, (c) voltages on primary and secondary capacitive couplers with $V_{in} = 100$ V.

For completeness, the variations of mutual capacitance with respect to different conditions of misalignment or air-gap is also experimentally investigated and depicted in Fig. 11. It was found that the value of C_M drops by 63% under 30-cm misalignment while reduced by 49% when the air-gap increases from 15 to 25 cm. As a result, the output power and system's efficiency are also decreased as illustrated in Fig. 12 and 13. However, the proposed CPT system can maintain efficiency above 76% even with a 30-cm misalignment or 25-cm air-gap. When metal plates perfectly aligned, then power transfer can be achieved at the rated value of 1.5-kW with the efficiency of 85.5 %. These results verify that the output power is proportional with C_M and the maximum output power is achieved at the highest value of C_M . As highlighted earlier, this is a beneficial feature enabling optimizing efficiency at high loads when the maximum output power is calculated at the highest value of the mutual capacitance. Furthermore, the output power cannot exceed the rated value of 1.5-kW if misalignment or air-gap variation occurs, thus the protection circuit is not necessary.

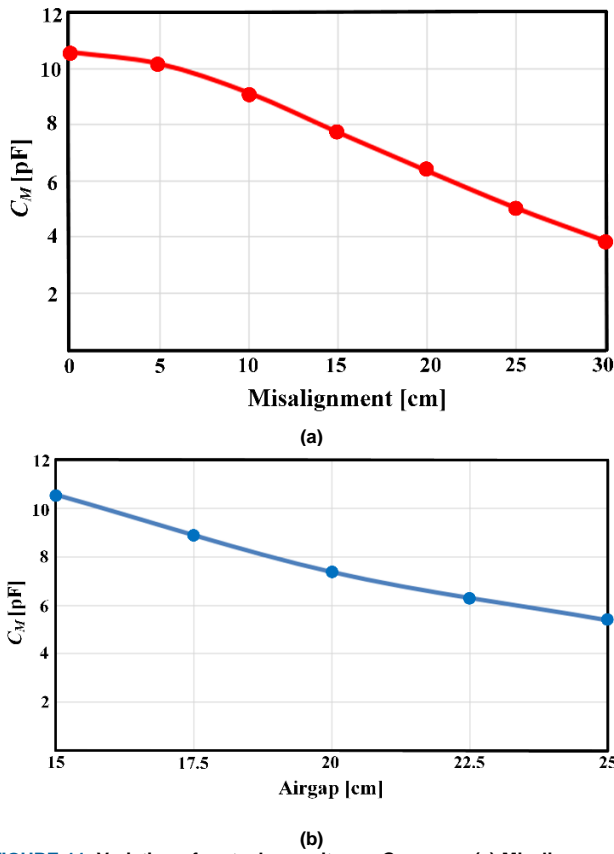


FIGURE 11. Variation of mutual capacitance C_M versus (a) Misalignments. (b) Different air-gap

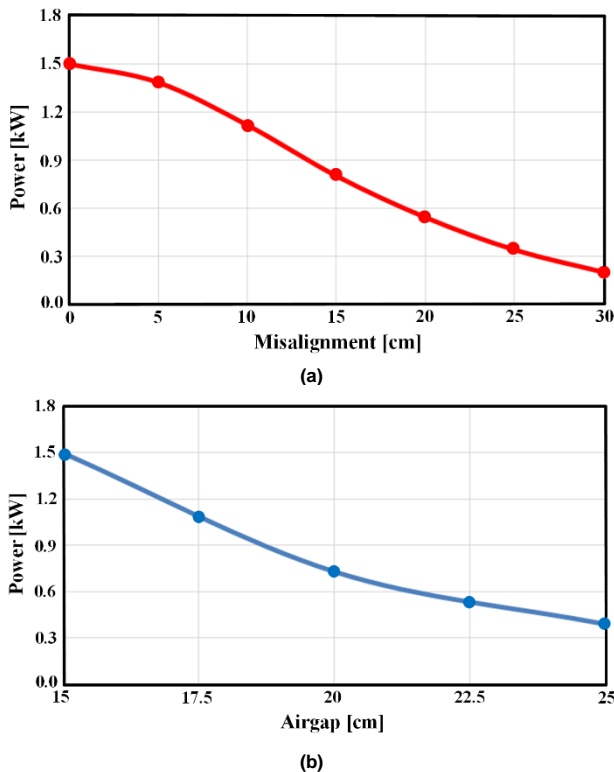


FIGURE 12. Output power and system's efficiency when $R_o = 10 \Omega$ according different conditions of (a) Misalignments. (b) Different air-gap

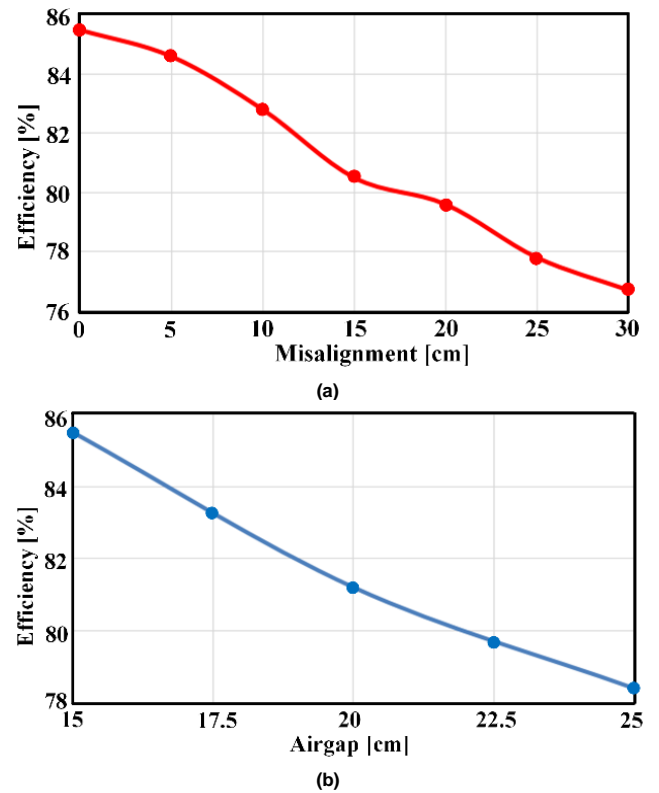


FIGURE 13. System's efficiency when $R_o = 10 \Omega$ according different conditions (a) Misalignments. (b) Different air-gap

The power loss distribution is estimated for the prototype based on the loss analysis for every single component. Detailed analysis is given in the APPENDIX. We consider the losses on the following components: inverter's switches, L_{1p} , C_{1p} , L_1 , capacitive coupler, L_2 and rectifier.

To reduce losses at an operating frequency of 1MHz, for all the inductors (L_{1p} , L_1 , L_2), the Litz wire (Litz wire-600 strands-AWG 38) is used while air-core is adopted. Moreover, the capacitor C_{1p} is constructed in parallel from several low-ESR capacitors from TDK to minimize the total resistance. The ESR value can be calculated based on the dissipation factor (DF) (i.e. $ESR = DF * \frac{1}{2\pi f C_{1p}}$). For Inverter switches, the switching loss is insignificant compared with conduction loss due to achieving ZVS turn on. At the secondary side, the loss on the rectifier is calculated based on the forward voltage of SiC Schottky Diodes. After all calculations, the remaining losses belong to the capacitive aluminium coupler. The loss distribution of the proposed converter is depicted in Fig. 14 with the total estimated loss of 218W at rated power. According to that aluminium coupler and resonant inductor L_2 contribute the highest losses which are 26.67% and 32.5% respectively. It can be explained that with the vertical structure coupler in Fig. 2b, there is an existing crossing coupling capacitive (i.e. C_{12} , C_{14} , C_{23} and C_{34}) which produces higher losses in the couplers. Moreover, the current on L_2 (i.e. same with output current I_o) is near twice the current on L_1 , therefore

producing double losses in inductor L_2 as compared to L_1 . Other components dissipate less than 18% of the total loss.

It is noted that there are no crossing capacitances in horizontal structure in [21] and therefore the associated losses with the coupler are reduced. Future works can be conducted by optimizing capacitive coupler to reduce the crossing capacitances effects and improve the system efficiency.

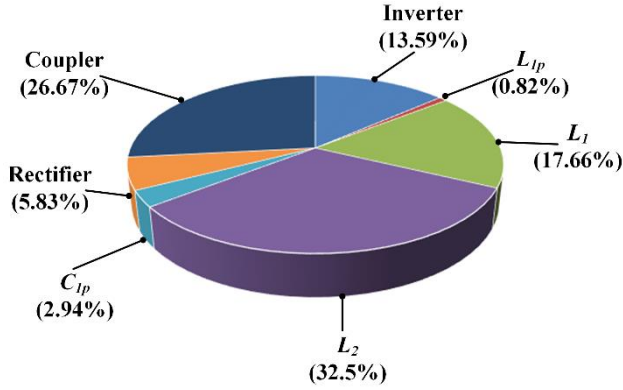


FIGURE 14. Power loss distribution of the proposed system components.

V. CONCLUSION

An improved LCL-L compensation circuit topology for a high-power CPT system is presented in this paper. An LCL compensation network is constructed at the primary side and an inductor is connected in series with the capacitive coupler at the secondary side. The proposed design enables achieving near ZPA operation and ZVS condition for primary inverter as well as the constant voltage between two primary capacitive couplers. Therefore, the output power is proportional to the coupling capacitance which brings several benefits in terms of design and overpower protection aspects. Furthermore, the number of external components is also minimized which helps to improve the system's compactness and reduce implementing cost. The proposed topology neglects almost drawbacks from previous CPT topologies and remains the good characteristics as mentioned before. Detailed analysis, design steps, and comparison are provided combining with simulated and experimental results to validate circuit topology. The proposed system can achieve an efficiency of 85.5% with 1.5-kW output power and a 150-mm air-gap.

APPENDIX

A. REFERENCES EQUATIONS DERIVATION OF LOSS CONTRIBUTIONS

This section investigates the power losses of every single component in the proposed converter. These calculations are mainly based on [29].

(1) The power conduction losses of the diode (P_{cond}) and MOSFET (P_{conMOS}):

$$P_{cond} = P_{cond} + P_{conMOS} = \frac{2\sqrt{2}}{\pi} V_{fws} I_{in} \left[1 - \sin\left(\frac{\varphi}{2}\right) \right] + \frac{1}{\pi} R_{ds} I_{in}^2 (\pi + \varphi + \sin \varphi) \quad (A1)$$

In which V_{fws} is the diode forward voltage, R_{ds} is the on-state resistance while φ and I_{in} are the conduction phase angle and output RMS current of the Inverter. In this work, φ is set as 175 degrees.

(2) The switching losses on MOSFET:

The switching losses can be represented in (A2): t_{ON} and t_{OFF} are the turn-on and turn-off times of MOSFET, I_D is the drain current of each switch while $V_{DS} = V_{in}$.

$$P_{swit} = 4V_{DS} I_D f_{SW} (t_{ON} + t_{OFF}) \quad (A2)$$

As analysis before, zero voltage switching at turn-on is achieved for the proposed converter (i.e. $t_{ON} = 0$), while the system is suffered from hard-switching at turn off. However, we can see the turn-off loss is not significant as the turn-off current is at small value of 3A (Fig. 8a). Therefore, switching losses are considered insignificant with the proposed system.

(3) Power losses on resonant network:

(a) On inductor L_{1p} , where R_{L1p} is the total AC and DC resistances of L_{1p} .

$$P_{loss_L1p} = I_{in}^2 R_{L1p} \quad (A3)$$

(b) On inductor L_1 , where R_{L1} is the total AC and DC resistances of L_1 . I_1 is the RMS value of current through the primary plate.

$$P_{loss_L1} = I_1^2 R_{L1} \quad (A4)$$

(c) On capacitor C_{1p} , where R_{C1p} is the total AC and DC resistances of C_{1p} .

$$P_{loss_C1p} = I_{C1p}^2 R_{C1p} \quad (A5)$$

(d) On inductor L_2 , where R_{L2} is the total AC and DC resistances of L_2 . I_1 is the RMS value of current through the primary plate.

$$P_{loss_L2} = I_1^2 R_{L2} \quad (A6)$$

All four resistance values of R_{L1p} , R_{L1} , R_{C1p} and R_{L2} can be estimated easily based on datasheets of Litz wire and capacitor. In experiments, these values have measured again by using the RLC meter.

(4) Conduction losses on rectifier: in the proposed system, secondary rectifier is built from SiC Schottky Diodes. The loss on the rectifier can be found in (A7) where V_{fwd} and r_D are the forward voltage and the On-State resistance of rectifier's diode.

$$P_{rec} = \frac{4\sqrt{2}}{\pi} V_{fwd} I_o + 2r_D I_o^2 \quad (A7)$$

(5) Losses on Aluminum capacitive coupler: it is difficult to determine exact loss on the coupler P_{Alu} . However, we can

estimate P_{Alu} after determining other component's losses. (A6) is the equation to determine P_{Alu} .

$$P_{Alu} = P_{total} - (P_{cond} + P_{swit} + P_{loss_{L1p}} + P_{loss_{L1p}} + P_{loss_{C1p}} + P_{loss_{L1p}} + P_{rec}) \quad (A8)$$

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